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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,534	05/12/2004	Bradley P. Jones	FIS920040035US1	3533

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EXAMINER
COLEMAN, WILLIAM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,534	JONES ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *May 12, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 May 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1A-1C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to because prior art figure 1C list element 118 which is not described in the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

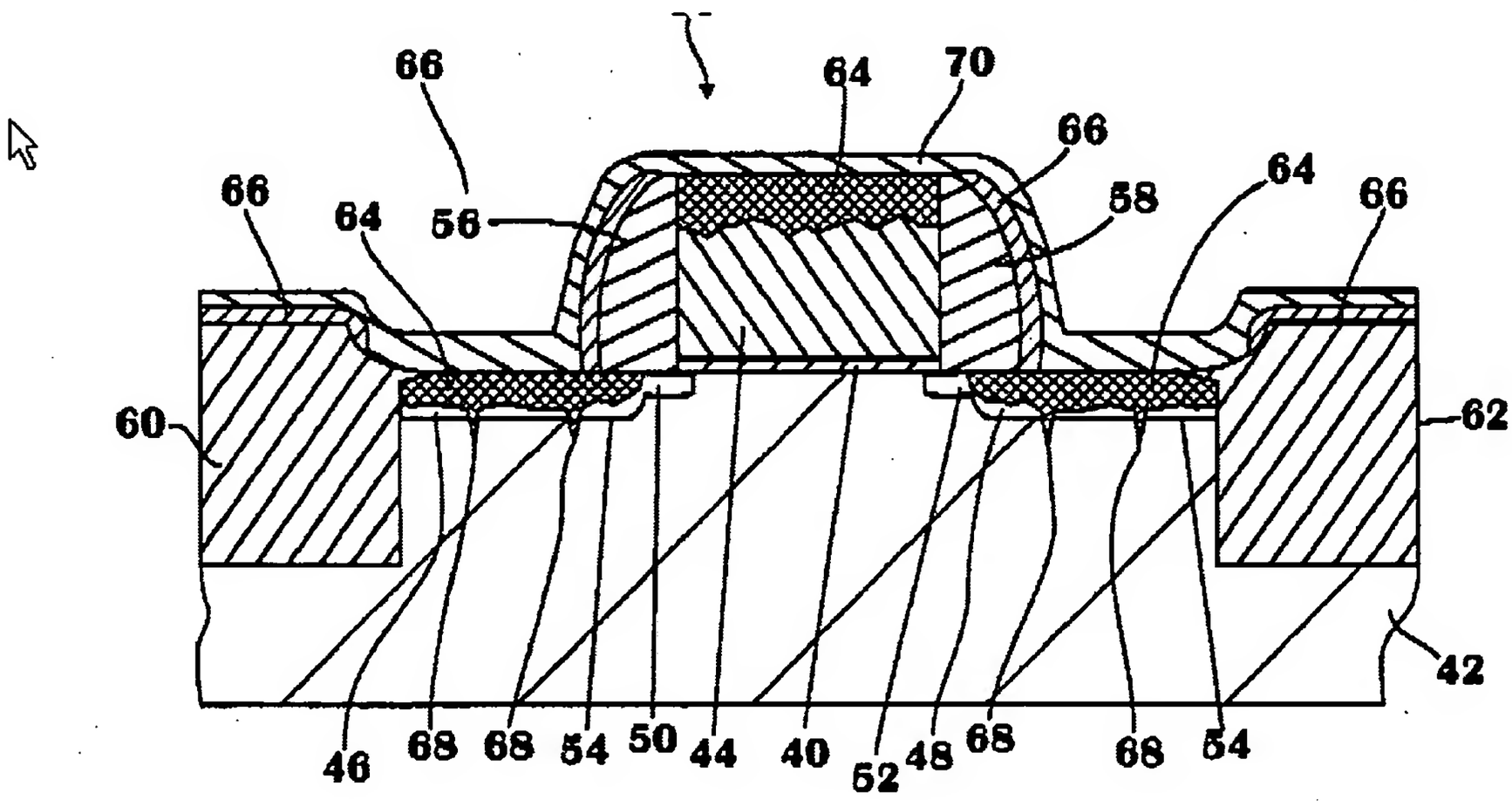
Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Wieczorek et al., U.S. Patent 6,207,563 B1.

Wieczorek discloses a semiconductor process as claimed. See FIGS. 1-7 and claims 1-39 where Wieczorek teaches the following limitations.



5. Pertaining to claim 1, Wieczorek teaches a method for reducing voiding between a first layer and a second layer formed over said first layer during a semiconductor annealing process, the method comprising:

forming a counter tensile layer over said second layer, wherein said counter tensile layer is selected from a material such that an opposing directional stress is created between said counter tensile layer and said second layer, with respect to a directional stress created between said first: layer and said second layer (see claims 21-39,)

6. Pertaining to claim 2, Wieczorek teaches the method of claim 1, wherein said counter tensile layer is selected to be the same material as said first layer.

7. Pertaining to claim 3, Wieczorek teaches the method of claim 2, wherein said first layer and said counter tensile layer comprise a refractory metal.

8. Pertaining to claim 4, Wieczorek teaches the method of claim 3, wherein said refractory metal comprises cobalt.

9. Pertaining to claim 5, Wieczorek teaches the method of claim 4, wherein said second layer comprises a titanium nitride cap layer.

10. Pertaining to claim 6, Wieczorek teaches a method for forming a metal silicide contact for a semiconductor device, the method comprising:

forming a refractory metal layer over a substrate, including active and non-active area of said substrate; forming a cap layer over said refractory metal layer; and forming a counter tensile layer over said cap layer, wherein said counter tensile layer is selected from a material such that

an opposing directional stress is created between said counter tensile layer and said cap layer, with respect to a directional stress created between said refractory metal layer and said cap layer.

11. Pertaining to claim 7, Wieczorek teaches the method of claim 6, wherein said counter tensile layer is selected to be the same material as said refractory layer.

12. Pertaining to claim 8, Wieczorek teaches the method of claim 7, wherein said refractory metal layer and said counter tensile layer comprise cobalt (column 6, line 50).

13. Pertaining to claim 9, Wieczorek teaches the method of claim 8, wherein said cap layer comprises a titanium nitride cap layer **70**.

14. Pertaining to claim 10, Wieczorek teaches the method of claim 6, wherein: said refractory metal layer is formed at a thickness of about 4 to about 7 nanometers;
said cap layer is formed at a thickness of about 10 to about 20 nanometers; and said counter tensile layer is formed at a thickness of about 10 to about 30 nanometers.

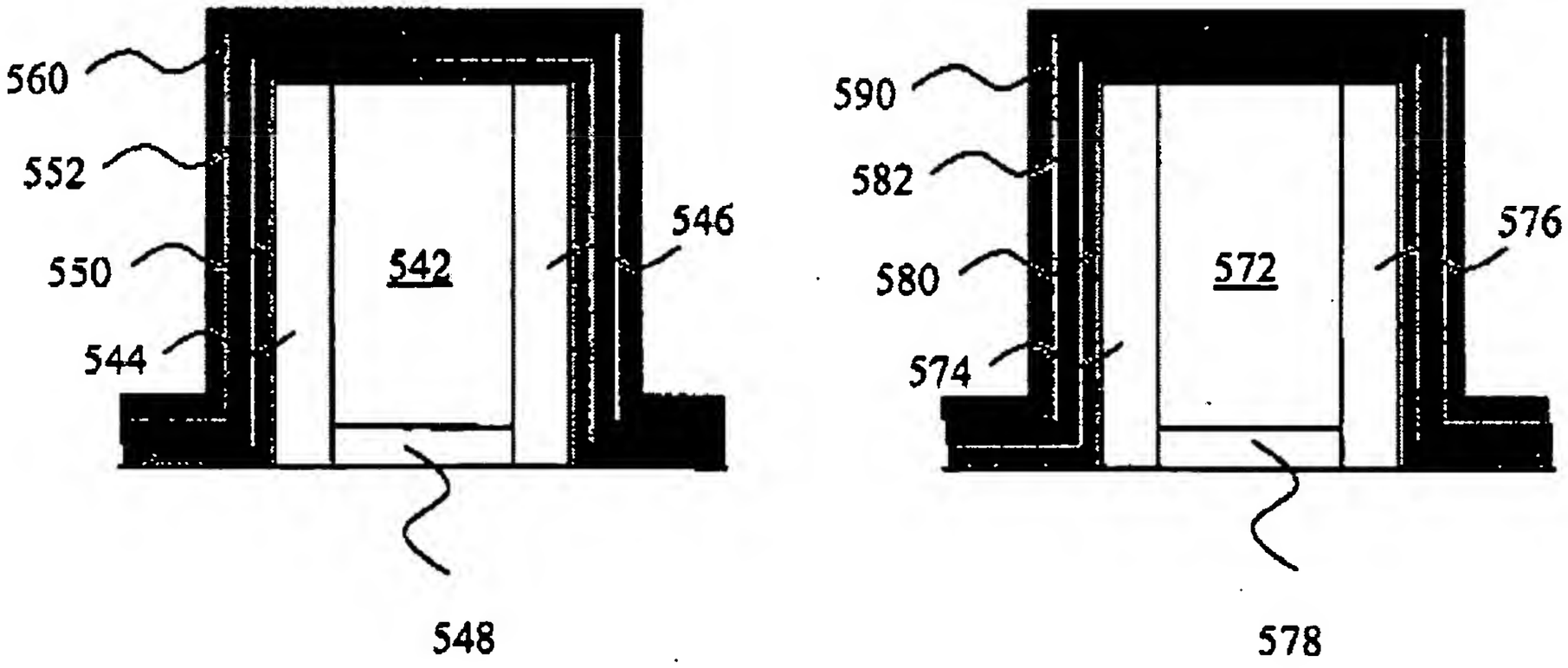
15. Pertaining to claim 11, Wieczorek teaches the method of claim 6, wherein: said refractory metal layer is formed at a thickness of about 4 to about 7 nanometers; said cap layer and said counter tensile layer are formed at a combined thickness of about 15 to about 30 nanometers.

16. Pertaining to claim 12, Wieczorek teaches the method of claim 6, further comprising annealing the substrate so as to cause portions of said refractory metal layer to react with active areas of said substrate.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

17. Claims 1, 2, 3, 4, 6, 7, 8 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al., U.S. Patent Application Publication US 2005/0156208 A1.

Lin discloses a semiconductor process as claimed. See FIGS 1-8K and in particular FIGS. 5a-5i where Lin teaches the claimed limitations.



18. Pertaining to claim 1, Lin teaches a method for reducing voiding between a first layer and a second layer formed over said first layer during a semiconductor annealing process, the method comprising:

forming a counter tensile layer **560** over said second layer **552**, wherein said counter tensile layer is selected from a material such that an opposing directional stress is created between said counter tensile layer and said second layer, with respect to a directional stress created between said first layer **550** and said second layer (cobalt/titanium/cobalt, see [0078]).

19. Pertaining to claim 2, Lin teaches the method of claim 1, wherein said counter tensile layer is selected to be the same material as said first layer.

20. Pertaining to claim 3, Lin teaches the method of claim 2, wherein said first layer and said counter tensile layer comprise a refractory metal.

21. Pertaining to claim 4, Lin teaches the method of claim 3, wherein said refractory metal comprises cobalt.

22. Pertaining to claim 6, Lin teaches a method for forming a metal silicide contact for a semiconductor device, the method comprising: forming a refractory metal layer over a substrate, including active and non-active area of said substrate; forming a cap layer over said refractory metal layer; and forming a counter tensile layer over said cap layer, wherein said counter tensile

layer is selected from a material such that an opposing directional stress is created between said counter tensile layer and said cap layer, with respect to a directional stress created between said refractory metal layer and said cap layer.

23. Pertaining to claim 7, Lin teaches the method of claim 6, wherein said counter tensile layer is selected to be the same material as said refractory layer.

24. Pertaining to claim 8, Lin teaches the method of claim 7, wherein said refractory metal layer and said counter tensile layer comprise cobalt.

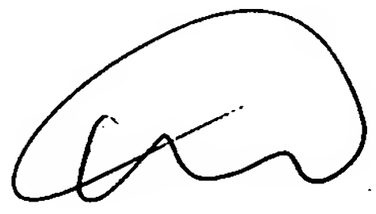
25. Pertaining to claim 12, Lin teaches the method of claim 6, further comprising annealing the substrate so as to cause portions of said refractory metal layer to react with active areas of said substrate.

Conclusion

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

28. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



W. David Coleman
Primary Examiner
Art Unit 2823

WDC